REMARKS

In accordance with the foregoing, claims 1, 5, 6, 12 and 16 have been amended and claims 1-8, 11-13, 15 and 16 are pending and under consideration.

Rejections under 35 USC § 102

On pages 2-8 of the September 22, 2005 Office Action, claims 1-8, 11-13, 15 and 16 were rejected under 35 USC § 102 as anticipated by U.S. Patent 5,930,508 to Faraboschi. The rejections are traversed below.

Claim 1 as amended recites a "parallel processor performing parallel processing of one or more basic instructions" (claim 1, lines 1-2) in which

> codes of the basic instructions are checked to identify the basic instructions, and the basic instructions, so identified, are associated with respective ones of said instruction execution units, said instruction execution units being associated with respective effective bits indicative of whether the basic instructions are supplied to said instruction execution units

(claim 1, 11-14). In other words, to determine which execution units are to execute the basic instructions, so that the identified basic instructions are associated with respective ones of the instruction execution units, codes of the basic instructions are checked to identify the basic instructions. Then, effective bits assigned in one-to-one correspondence with the instruction execution units are used to indicate whether the basic instructions are supplied to the instruction execution units.

In contrast, what was cited in Faraboschi describes a very long instruction word (VLIW) "processor having multiple functional units ... for storing compacted instructions ... and a dispersal circuit transfers each word of the compacted instruction" (Abstract, lines 2-12); Faraboschi further describes storing "instruction words with significant numbers of NOPs [No Op Codes] in memory is wasteful of memory space" (column 1, lines 51-65) in describing FIG. 1. Faraboschi also describes compensation for increases in interconnect wires and increased chip area required by "dispersement logic 600 shown in FIG. 6" (column 7, lines 44-46) in referring to FIG. 7. (see, column 7, lines 17-48). Faraboschi also describes "interleaved" dispersement logic, i.e., a "compacted instruction in bit interleaved format is read out of instruction cache 910, aligned in bit interleaved format" (column 9, line 1-12; referring to FIG. 9). In other words, what was cited in Faraboschi teaches selecting an execution unit for execution of an instruction by use of a dispersal bit set. As shown in FIGS. 4 and 5, each syllable in a compacted instruction has an associated dispersal bit set, which indicates the functional unit by which the syllable is to

be executed. The dispersal block shown in FIG. 6 transforms the compacted instruction into a dispersed instruction by using the dispersal bit sets.

The difference between claim 1 and the processor disclosed in Faraboschi is that a dispersal bit set is not used for specifying the execution unit to execute a basic instruction. Instead, the code of a basic instruction is checked (decoded) to identify a corresponding execution unit. As a result, a larger number of bits of an instruction word can be utilized for instruction code fields without requiring dispersal bit sets as taught by Faraboschi. For example, Applicants' invention can properly select execution units without the need to provide every single one of the basic instructions (syllables) with information indicative of which one of the execution units is to be used. The present claimed invention is not anticipated by Faraboschi because Faraboschi fails to teach or suggest each element of the claimed invention. Thus, for the reasons discussed above, claim 1 is in condition for allowance.

Independent claim 16 recites limitations similar to those discussed above with respect to claim 1 and adds explicitly that "instruction word[s] ... have no attached dispersal information" (claim 16, lines 11-12). Dependent claims 2-8, 11-13 and 15 depend from claim 1 and subsequent base claims. Thus, claims 2-8, 11-13, 15 and 16 distinguish over the applied art for reasons discussed in regard to claim 1.

CONCLUSION

It is submitted that the applied art cited by the Examiner does not teach or suggest the features of the present claimed invention. Thus, it is submitted that claims 1-8, 11-13, 15 and 16 are in a condition suitable for allowance. Reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Finally, if there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
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